

Appl. No. 09/975,444  
Reply to Office action of 05/20/2003

Amendments to the Claims:

Claims 1-11: (canceled).

Claim 12: (currently amended) A method of fabricating an integrated circuit, comprising the steps of:

    forming a dielectric layer over a semiconductor body;  
    forming a trench in a first part of said dielectric layer;  
    forming a via in a second part of said dielectric layer;  
    depositing a liner/barrier layer over said dielectric layer including in said trench and in said via using physical vapor deposition (PVD);  
    performing a sputter etch using a low bias after said step of depositing a liner/barrier layer;  
    depositing a seed layer over said liner/barrier layer after said step of performing the sputter etch; and  
    depositing a copper layer over said seed layer.

Claim 13: (original) The method of claim 12, wherein said step of depositing a seed layer comprises PVD and occurs prior to said step of performing a sputter etch.

Claim 14: (original) The method of claim 12, wherein said steps of forming the liner/barrier layer and forming the seed layer create an overhang portion of liner/barrier and seed material and wherein said sputter etch step reduces thickness of said overhang portion.

Claim 15: (original) The method of claim 12, wherein said liner/barrier layer comprises a material selected from the group consisting of Ti, TiN, Ta, TaN, TiNSi, WN, TaNSi, MoN.

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Claim 16: (original) The method of claim 12, wherein said low bias is in the range of 0 to -300 volts.

Claim 17: (currently amended) A method of fabricating an integrated circuit, comprising the steps of:

forming a pre-metal dielectric (PMD) layer over a semiconductor body;

forming a contact hole in said PMD layer;

depositing a liner layer over said PMD layer including in said contact hole using physical vapor deposition, wherein said liner layer has an overhang portion at a top of said contact hole;

performing a sputter etch using a low bias to at least reduce a thickness of said overhang portion after said step of depositing the liner layer;

depositing a barrier layer over said liner layer after said step of performing a sputter etch; and

depositing a metal filler to fill said contact hole.

Claim 18. (original) The method of claim 17, wherein said step of depositing a barrier layer comprises PVD and occurs prior to said step of performing a sputter etch.

Claim 19. (original) The method of claim 17, wherein said metal filler comprises tungsten.

Claim 20. (original) The method of claim 17, wherein said metal filler comprises CVD TiN.

Claim 21. (original) The method of claim 17, wherein said liner layer comprises Ti and barrier layer comprises TiN.

Claim 22. (original) The method of claim 17, wherein said low bias is in the range of 0 to -300 volts.